Claims

[c1] 1.A split-gate fin-type field effect transistor (FinFET) comprising:
a plurality of parallel fin structures;
back gate conductors between channel regions of alternating pairs of said fin structures; and
front gate conductors between channel regions of opposite alternating pairs of said fin structures.

[c2] 2.The split-gate FinFET in claim 1, further comprising:
a back gate wiring layer connected to said back gate conductors;
a front gate wiring layer connected to said front gate conductors;
a first insulator layer positioned between said front gate conductors and said back gate wiring layer; and
a second insulator layer positioned between said back gate conductors and said front gate wiring layer.

[c3] 3.The split-gate FinFET in claim 2, further comprising:
a first conductive via connected to said back gate wiring layer; and
a second conductive via connected to said front gate wiring layer.

[c4] 4.The split-gate FinFET in claim 2, wherein said front gate conductors and said front gate wiring layer comprise a continuous conductive unitary structure.

[c5] 5.The split-gate FinFET in claim 1, wherein ones of said front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of said split gate FinFET.

[c6] 6.The split-gate FinFET in claim 1, further comprising gate insulators between said back and front gate conductors and said channel regions.

[c7] 7.The split-gate FinFET in claim 1, wherein said back gate controls the threshold voltage level of said split-gate FinFET.

[c8] 8.A split-gate fin-type field effect transistor (FinFET) comprising:
a plurality of parallel fin structures, wherein each of said fin structures comprises a source region in a first end of said fin, a drain region in a second end of said fin, and a channel region in a middle portion of said fin between said first end and said second end;
back gate conductors between channel regions of alternating pairs of said fin structures;
front gate conductors between channel regions of oppo-

site alternating pairs of said fin structures, such that said back gate conductors and said front gate conductors are alternatively interdigitated between channel regions of said fin structures and such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure;

a well region positioned below said fin structures, wherein said well region is electrically connected to said back gate conductors; and

a front gate wiring layer positioned above said fin structures, wherein said front gate wiring layer is electrically connected to said front gate conductors.

[c9] 9.The split-gate FinFET in claim 8, further comprising:

a first insulator layer positioned between said well region and said front gate conductors; and

a second insulator layer positioned between said front gate wiring layer and said back gate conductors.

[c10] 10.The split-gate FinFET in claim 8, further comprising:

a first conductive via connected to said well region; and

a second conductive via connected to said front gate wiring layer.

[c11] 11.The split-gate FinFET in claim 8, wherein said front gate conductors and said front gate wiring layer com-

prise a continuous conductive unitary structure.

[c12] 12.The split-gate FinFET in claim 8, wherein ones of said front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of said split gate FinFET.

[c13] 13.The split-gate FinFET in claim 8, further comprising gate oxides between said back and front gate conductors and said channel regions.

[c14] 14.The split-gate FinFET in claim 8, wherein said back gate controls the threshold voltage level of said split-gate FinFET.

[c15] 15.A split-gate fin-type field effect transistor (FinFET) comprising:
a plurality of parallel fin structures, wherein each of said fin structures comprises a source region in a first end of said fin, a drain region in a second end of said fin, and a channel region in a middle portion of said fin between said first end and said second end;
back gate conductors between channel regions of alternating pairs of said fin structures;
front gate conductors between channel regions of opposite alternating pairs of said fin structures, such that said back gate conductors and said front gate conductors are

alternatively interdigitated between channel regions of said fin structures and such that each of said channel regions has a back gate conductor on one side of each fin structure and a front gate conductor on the other side of said fin structure;

a back gate wiring layer positioned below said fin structures, wherein said back gate wiring layer is electrically connected to said back gate conductors; and

a front gate wiring layer positioned above said fin structures, wherein said front gate wiring layer is electrically connected to said front gate conductors.

[c16] 16.The split-gate FinFET in claim 15, further comprising:

a first insulator layer positioned between said back gate wiring layer and said front gate conductors; and

a second insulator layer positioned between said front gate wiring layer and said back gate conductors.

[c17] 17.The split-gate FinFET in claim 15, further comprising:

a first conductive via connected to said back gate wiring layer; and

a second conductive via connected to said front gate wiring layer.

[c18] 18.The split-gate FinFET in claim 15, wherein said front gate conductors and said front gate wiring layer comprise a continuous conductive unitary structure.

[c19] 19.The split-gate FinFET in claim 15, wherein ones of said front gate conductors are positioned adjacent to outer sides of channel regions of end fin structures of said split gate FinFET.

[c20] 20.The split-gate FinFET in claim 15, further comprising gate insulators between said back and front gate conductors and said channel regions.

[c21] 21.The split-gate FinFET in claim 15, wherein said back gate controls the threshold voltage level of said split-gate FinFET.

[c22] 22.A method of forming a split-gate fin-type field effect transistor (FinFET), said method comprising:
providing a laminated structure having a semiconductor layer;
patterning openings in said semiconductor layer;
filling said openings with a back gate conductor to form a plurality of back gate conductors;
patterning said semiconductor layer into fins, such that a fin is positioned adjacent each side of said back gate conductors, wherein said patterning leaves one side of each fin exposed;
depositing a front gate conductor over exposed portions of said fins, such that each of said fins has a front gate

conductor on a first side and a back gate conductor on a second side; and

simultaneously patterning said back gate conductors and said front gate conductor into linear gate conductors intersecting said fins.

[c23] 23.The method in claim 22, wherein said patterning of said openings forms said openings through an insulator layer below said semiconductor layer to a back gate wiring layer below said insulator layer in said laminated structure.

[c24] 24.The method in claim 23, further comprising forming conductive vias to said front gate conductor and to said back gate wiring layer.

[c25] 25.The method in claim 22, wherein said process of simultaneously patterning said back gate conductors and said front gate conductor automatically aligns said back gate conductors with said front gate conductor.

[c26] 26.The method in claim 22, wherein said laminated structure comprises a silicon-on-insulator (SOI) and said back gate conductor controls the threshold voltage level of said FinFET.

[c27] 27.The method in claim 22, further comprising forming first insulators that electrically separate said back gate

conductors from said front gate conductor.

[c28] 28.The method in claim 22, wherein said patterning of said openings comprises patterning parallel rectangular openings in said semiconductor layer.

[c29] 29.A method of forming a split-gate fin-type field effect transistor (FinFET), said method comprising:
providing a laminated structure having a semiconductor layer;
patterning openings in said semiconductor layer;
forming back gate insulators on exposed portions of said semiconductor layer within said openings;
filling said openings with a back gate conductor to form a plurality of back gate conductors;
forming first insulators above said back gate conductor;
patterning said semiconductor layer into fins, such that a fin is positioned adjacent each side of said back gate conductors, wherein said patterning leaves one side of each fin exposed;
forming front gate insulators on exposed portions of said fins;
depositing a front gate conductor over exposed portions of said fins and said first insulators, such that each of said fins has a front gate conductor on a first side and a back gate conductor on a second side;
simultaneously patterning said back gate conductors and

said front gate conductor into linear gate conductors intersecting said fins, wherein said patterning of said back gate conductors and said front gate conductor is selective to said fins, such that ends of said fins are exposed after said patterning of said back gate conductors and said front gate conductor; and
doping said ends of said fins to form source and drain regions.

[c30] 30.The method in claim 29, wherein said patterning of said openings forms said openings through an insulator layer below said semiconductor layer to a back gate wiring layer below said insulator layer in said laminated structure.

[c31] 31.The method in claim 30, further comprising forming conductive vias to said front gate conductor and to said back gate wiring layer.

[c32] 32.The method in claim 29, wherein said process of simultaneously patterning said back gate conductors and said front gate conductor automatically aligns said back gate conductors with said front gate conductor.

[c33] 33.The method in claim 29, wherein said laminated structure comprises a silicon-on-insulator (SOI) and said back gate conductor controls the threshold voltage level

of said FinFET.

[c34] 34.The method in claim 29, wherein said first insulators electrically separate said back gate conductors from said front gate conductor.

[c35] 35.The method in claim 29, wherein said patterning of said openings comprises patterning parallel rectangular openings in said semiconductor layer.

[c36] 36.A method of forming a split-gate fin-type field effect transistor (FinFET), said method comprising:
providing a laminated structure having a semiconductor layer;
patterning openings in said semiconductor layer;
filling said openings with a back gate conductor to form a plurality of back gate conductors;
patterning said semiconductor layer into fins, such that a fin is positioned adjacent each side of said back gate conductors, wherein said patterning leaves one side of each fin exposed;
depositing a front gate conductor over exposed portions of said fins, such that each of said fins has a front gate conductor on a first side and a back gate conductor on a second side; and
simultaneously patterning said back gate conductors and said front gate conductor into linear gate conductors in-

tersecting said fins, wherein said patterning of said openings forms said openings through an insulator layer below said semiconductor layer to a well region below said insulator layer in said laminated structure.

[c37] 37.The method in claim 36, further comprising forming conductive vias to said front gate conductor and to said diffusion region.

[c38] 38.The method in claim 36, wherein said process of si- multaneously patterning said back gate conductors and said front gate conductor automatically aligns said back gate conductors with said front gate conductor.

[c39] 39.The method in claim 36, wherein said laminated structure comprises a silicon-over-insulator (SOI) and said back gate conductor controls the threshold voltage level of said FinFET.

[c40] 40.The method in claim 36, further comprising forming first insulators that electrically separate said back gate conductors from said front gate conductor.

[c41] 41.The method in claim 36, wherein said patterning of said openings comprises patterning parallel rectangular openings in said semiconductor layer.